REMARKS/ARGUMENTS

Reconsideration of the rejections set forth in the Office Action dated December 31, 2003 is respectfully requested. Claims 1-44 have been rejected, and claims 45-48 have been added. As such, claims 1-48 are currently pending.

Claim 7 has been amended to correct an inconsistency in dependency. New claims 45-48 are apparatus claims which are similar in scope to those already presented.

Rejections under 35 U.S.C. § 103

The Examiner has rejected claims 1-4, 7, 9-11, 13, 15-17, 18, 22, 35, and 36 under 35 U.S.C. § 103(a) as being anticipated by Smith (U.S. Patent No. 6,188,686) in view of Laor et al. (U.S. Patent No. 6,424,649). The Examiner has rejected claim 5 under 35 U.S.C. § 103(a) as being unpatentable over Smith (U.S. Patent No. 6,188,686) in view of Laor et al. (U.S. Patent No. 6,424,649) further in view of Demiray et al. (U.S. Patent No. 5,740,157). Claims 6 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Smith in view of Laor et al. further in view of Lamarche et al. (U.S. Patent No. 6,414,953). Claims 12, 14, 20, 21, 23, and 24 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Smith in view of Laor et al. further in view of Tarridec et al. (U.S. Patent No. 4,751,699). Claim 19 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Smith in view of Laor et al. further in view of Upp et al. (U.S. Patent No. 5,967,405). Claims 25-34 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Smith in view of Laor et al. further in view of Kosugi et al. (U.S. Patent No. 5,189,410). Claims 37 and 40-44 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Smith in view of Laor et al. further in view of Madonna (U.S. Patent No. 5,737,320).

1. Independent claim 1 and its dependents

Independent claim 1 requires an apparatus which includes a plurality of interface cards, a cross-connect unit, a control unit, and a backplane forming parallel data buses. The parallel data buses include a clock recovered parallel data bus that provides connectivity between each of a plurality of interface cards, the cross-connect unit, and the control unit. Data streams are transmitted between the plurality of interface cards and the cross-connect unit over the clock recovered parallel data bus without synchronization information.

In his rejections, the Examiner has stated that Smith in view of Laor et al. discloses the apparatus as claimed in claim 1. The Applicants respectfully submit that neither Smith nor Laor et al. alone or in combination, appear to teach of a clock recovered parallel data bus or of transmitting data streams without synchronization information. In the Office Action dated December 31, 2003, the Examiner has acknowledged that Smith does not expressly disclose a clock recovered bus without synchronization information, but argues that "Laor et al. disclosers a switch that operates asynchronously, but appears to operate synchronously by using a single clock signal source which is uniform for the switch interconnect...." (Office Action dated December 31, 2003, page 3). The Examiner further argues that Laor et al. teach of a phase locked loop used for synchronization purposes so that synchronization information does not have to be sent in packets.

The Applicants respectfully disagree with the Examiner's arguments. While Laor et al. appears to teach that a phase locked loop synchronizes to a single frequency source (Laor et al., column 1, lines 61-67), as noted by the Examiner, a phase locked loop that synchronizes to a single frequency source does not show or reasonably suggest that data streams are sent over a clocked recovered parallel data bus without synchronization information. The phase locked loop of Laor et al. does not appear to be a clock recovered data bus, and there is no suggestion in Laor et al. that data steams are sent without synchronization information. Since claim 1 requires a clock recovered data bus, claim 1 is believed to be allowable over the art of record for at least this reason.

It is submitted that a phase locked loop as taught by Laor et al. which synchronizes to a

single frequency source does not imply that phase locked loops are used so that synchronization information does not have to be sent, as alleged by the Examiner. There appears to be no suggestion of not sending synchronization information in Laor et al. Even if it is assumed that a phase locked loop does not use any synchronization information from data to synchronize, there is still no teaching or suggestion in Laor et al. that synchronization information is not included in a data stream. The information may still be included in the data stream, since Laor et al. does not teach or suggest that the information is not included in the data stream. As Laor et al. does not appear to teach of, or even suggest, sending data streams without synchronization information, claim 1 is also believed to be allowable over the art of record for at least this reason as well.

Claims 2-34 each depend either directly or indirectly from independent claim 1, and are therefore each believed to be allowable over the art of record for at least the reasons set forth above with respect to independent claim 1. Each of these independent claims recites additional limitations which, when considered in view of claim 1, are believed to further distinguish the claimed invention over the art of record. By way of example, dependent claim 18 requires that a first set of interface subsystems supported by a first set of interface cards forms a telecommunications plane, and that a second set of interface subsystems supported by a second set of interface cards forms a data plane. The Examiner has argued that "grouping a first set of ports together could form one plane, while grouping a second set of interfaces together would form a second plane " (Office Action dated December 31, 2003, page 4). It is respectfully submitted that there is no teaching or suggestion in any of the art of record of grouping interface subsystems. Further, none of the art of record makes any mention of interface subsystems being grouped specifically into a telecommunications plane and a data plane. Therefore, claim 18 is believed to be allowable over the cited art for at least this reason as well.

The Applicants are unable to identify a rejection for claim 8, although the Examiner has indicated that claim 8 has been rejected. As such, the Applicants would like to request that the Examiner provide a reason for his rejection of claim 8, so that the Applicant may more properly respond to the rejection of claim 8. It is noted, however, that neither Smith nor Laor et al. appears to show or suggest a backplane that connects each of a plurality of card slots to all other card slots so that a first card can communicate with a second card regardless of the location of

the cards. By way of example, Laor et al. specifically teaches of input and output interface cards (Laor et al., FIG. 1 and corresponding description). Hence, it is respectfully submitted that a card designated as an output card by Laor et al. would not communicate with another card designated as an output card.

2. Independent claim 35 and its dependent

Independent claim 35 requires that an apparatus includes a plurality of clock recoverable interface cards for transmitting and receiving data streams having no synchronization information and a plurality of clocked interface cards for transmitting and receiving data streams including data and synchronization information. The apparatus also includes a backplane forming parallel data buses including clock recovered parallel data buses and clocked parallel buses that provide connectivity between the interface cards, a cross-connect unit, and a control unit.

It is respectfully submitted that neither Smith nor Laor et al., alone or in combination, appear to teach or show an apparatus with a plurality of clock recoverable interface cards for transmitting and receiving data streams having no synchronization information and a plurality of clocked interface cards for transmitting and receiving data streams including data and synchronization information. Smith states that data units may operate asynchronously (Smith, column 5, line 55), but does not teach or suggest that a plurality of clock recoverable interface cards and a plurality of clocked interface cards be included in an apparatus. Further, Smith does not appear to teach of an apparatus which includes both a plurality of clock recoverable interface cards for transmitting and receiving data streams having no synchronization information and a plurality of clocked interface cards for transmitting and receiving data streams including data and synchronization information.

As discussed above, Laor et al. appears to teach that a phase locked loop synchronizes to a single frequency source (Laor et al., column 1, lines 61-67). It is respectfully submitted, however, that a phase locked loop that synchronizes to a single frequency source does not show or reasonably suggest a plurality of clock recoverable interface cards for transmitting and receiving data streams having no synchronization information. The switch with a phase locked loop, as taught by Laor et al., does not appear to be a clock recoverable interface card for

transmitting and receiving data streams having no synchronization information. In the art of record, there does not appear to be any mention of or suggestion of transmitting and receiving data streams having no synchronization information. Accordingly, claim 35 and its dependent are believed to be allowable over the art of record for at least this reason.

It is further submitted that Laor et al. does not teach of or suggest a plurality of clock recovered interface cards. In addition, no combination of the art of record appears to teach of or suggest a backplane forming parallel data buses including clock recovered parallel data buses and clocked parallel data buses, as taught in claim 35. Smith does not teach of either clock recovered parallel data buses or clocked parallel data buses. Laor et al. also does not appear to teach of a clock recovered parallel data bus, or of a backplane which includes both a clock recovered parallel data bus and a clocked parallel data bus. As such, claim 35 and its dependent are also believed to be allowable over the art of record for at least this reason as well.

Independent claim 37 requires that a method for flexibly transmitting telecommunications signals includes receiving a first payload, removing a first telecommunications signal from the first payload and inserting the telecommunications signal in a second payload, and transmitting the second payload. The first and second payloads do not include synchronization information and are transmitted over a clock recovered parallel data bus formed in a backplane of a cross-connect apparatus.

3. Independent claim 37 and its dependents

With regards to claim 37, the Examiner has argued that Smith in view of Laor et al. further in view of Madonna teaches the claimed limitations. It is respectfully submitted that, as discussed above with reference to claim 1, Smith in view of Laor et al. does not teach of signals or payloads which do not include synchronization information, and does not teach of a clock recovered parallel data bus or of transmitting signals over a clock recovered parallel data bus. Madonna also does not appear to teach of payloads which do not include synchronization information, or of a clock recovered parallel data bus. As such, claim 37 is believed to be allowable over the art of record for at least these reasons.

Madonna appears to teach of sending an empty packet from a first node to a second node, and inserting local circuit switched data pertaining to the second node into the empty packet (Madonna, column 14, lines 13-54). Madonna also appears to teach of sending a full packet, full of information pertaining to a first node, from the first node to a second node, and extracting data from the payload at the second node (Madonna, from column 14 at line 55 to column 15 at line 7). On page 8 of the Office Action dated December 31, 2003, the Examiner has argued that information extracted from a full packet may subsequently be placed into an empty packet. The information extracted from a full packet is information associated with an originating node (Madonna, column 14, lines 62-64), and the information placed into an empty packet pertains to a receiving node (Madonna, column 14, lines 29-32). Since Madonna appears to teach that a first node, when sending a full packet, includes only information relating to the first node (in the packet) and also appears to teach that a second node, when receiving an empty packet, only places information relating to the second node in the packet, in the system of Madonna, information extracted from the full packet by the second node does **not** pertain to the second node and, hence will not be written by the second node into an empty packet. As such, the Applicants respectfully submit that no combination of Smith, Laor et al., or Madonna, either alone or in combination, teaches of removing a first telecommunications signal from a first payload and inserting the first telecommunications signal in a second payload before transmitting the second payload. As such, claim 37 is further believed to be allowable over the art of record for at least this additional reason.

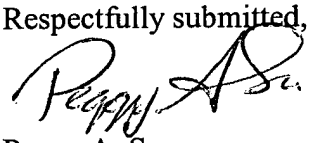
Claims 38-44 each depend either directly or indirectly from independent claim 37 and are, hence, each believed to be allowable over the art of record for at least the reasons set forth above with respect to claim 37.

4. Conclusion

In view of the above, the Applicants believe that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

If any fees are due in connection with the filing of this amendment, the Commissioner is authorized to charge such fees to Deposit Account 50-1652 (Order No. CISCP793).

Respectfully submitted,



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